UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,652	12/13/2001	Taeyoun Kwon	671-10 (P9936)	2016

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ART UNIT	PAPER NUMBER
2617	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/020,652	KWON, TAEYOUN
	Examiner	**Art Unit**	
	Sam Bhattacharya	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 October 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,11-13 and 15* is/are rejected.

7)☒ Claim(s) *6-10 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beckert et

al. (US 6,862,651) in view of Brown, III et al. (US 6,038,636).

Regarding claims 1 and 3, Beckert et al. discloses a mobile communication device that

includes a flash memory 402 for storing program data and user data, an interface circuit 414 over

which data is copied from the flash memory, a first RAM 404 for providing an operation area to

store and execute the copied program data from the flash memory, and a second RAM 406 for

storing data generated during the execution of the program data, wherein the first and second

RAMs are independent memories. See FIG. 4, col. 22, lines 9-35, col. 23, lines 8-38 and col. 24,

lines 20-32.

Beckert et al. fails to disclose copying program data stored in the flash memory according

to whether data stored in the flash memory is valid.

In an analogous art, Brown, III et al. disclose a method of reclaiming and defragmenting

a flash memory device in which data is copied from the flash memory to another memory based

on whether it is valid. See col. 3, lines 28-49. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the mobile communication

device of Beckert et al. by incorporating these teachings of Brown, III et al. for the purpose of

restoring only valid files to the flash memory in their original format.

3.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beckert et al. in

view of Brown, III et al. and Costello et al. (US 6,754,894).

The Beckert-Brown combination fails to disclose a flash memory that is a NAND-type

type flash memory.

However, in an analogous art, Costello et al. discloses a mobile communication device

that includes a NAND-type flash memory 512 that stores program data and user data. See FIG. 5

and col. 6, lines 5-32. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to modify the mobile communication device of Beckert et al.

and Brown, III et al. by incorporating this feature taught in Costello et al. for the purpose of

achieving a larger memory space and faster memory speeds.

4.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beckert et al. in

view of Brown, III et al. and Christopherson et al. (US 5,475,693).

Regarding claim 4, Beckert in view of Brown fails to disclose that the interface circuit is

an ASIC including a ROM for storing program codes and an error correction circuit.

However, Christopherson discloses error management processes for flash EEPROM

memory arrays including a memory device 16 (in FIG. 1) for affecting an accuracy of data

provided by a flash memory comprising a flash memory 23 (in FIG. 2), an interface circuit (20,

22, 25, 26, 27 and 28) for implementing and coordinating the various operations of the memory

device, wherein element 22 is an AISC including error correction circuit (55 and 56, figure 2, and col. 3 lines 53-58) and element 27 is a ROM. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the mobile communication device of Beckert and Brown by incorporating these teachings in Christopherson for the purpose of providing a smaller, faster and less expensive interface circuit.

5.   Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beckert et al. in view of Brown, III et al. and Niiyama et al. (US 5,400,389).

Regarding claim 5, the combination of Beckert and Brown fails to disclose a mobile communication device that includes an interface circuit that generates a chip enable signal enabling the flash ROM.

However, Niiyama et al. discloses mobile communication device that includes an interface circuit 506 that generates a chip enable signal enabling the flash ROM 502. See col. 6, lines 11-18. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the mobile communication device of Beckert et al. and Brown, III et al. by sending a chip enable signal from the interface circuit to the flash memory as taught by Niiyama et al. to activate the flash memory in association with an address supplied from the microprocessor.

6.   Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Costello et al. (US 6,754,897) in view of Christopherson et al.

Regarding claim 11, Costello discloses a mobile communication device that includes an analog circuit 502 for air interfacing the mobile communication device, a user interface circuit (indicated as a "display device") for interfacing between the mobile communication device and a user, a microprocessor 504 for providing overall control of the operation of the mobile device, and a memory device including a flash memory 512 for storing program data and user data, a first memory 508 for copying the program data of the flash memory, and a second memory 510 for executing the program data of the first memory, wherein the first and second memories are independent memories. Moreover, it is inherent to the device of Costello et al. to include an interface circuit for interfacing the flash memory to the microprocessor. See FIG. 5, col. 6, lines 5-22, lines 44-67, and col. 7, lines 24-34.

Costello fails to disclose that the interface circuit is an ASIC including a ROM for storing program codes and an error correction circuit.

However, Christopherson discloses error management processes for flash EEPROM memory arrays including a memory device 16 (in FIG. 1) for affecting an accuracy of data provided by a flash memory comprising a flash memory 23 (in FIG. 2), an interface circuit (20, 22, 25, 26, 27 and 28) for implementing and coordinating the various operations of the memory device, wherein element 22 is an AISC including error correction circuit (55 and 56, figure 2, and col. 3 lines 53-58) and element 27 is a ROM. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the mobile communication device of Costello by incorporating these teachings in Christopherson for the purpose of providing a smaller, faster and less expensive interface circuit.

Regarding claim 12, Costello et al. discloses a flash memory that is a NAND-type flash memory. See col. 6, line 32.

7.   Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Costello in view of Chistopherson and Niyama et al.

Regarding claim 13, Costello discloses that the first memory 508 and the second memory 510 are NOR flash and RAM memories, respectively. However, Costello and Chistopherson fail to disclose both first and second memories that are RAM memories.

Niiyama et al. discloses a mobile communication device that includes a microprocessor 501, a ROM 502 (which can be a flash ROM), and first and second RAMs 503 and 504. The microprocessor controls the operations of the RAMs according to an operation program stored in the flash ROM. See FIG. 4 and col. 5, line 62 - col. 6, line 29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the mobile communication device of Costello and Christopherson by using first and second RAM memories as taught by Niiyama et al. to attain faster speeds of access and execution for data and programs stored in the memories.

Regarding claim 15, Niiyama et al. discloses mobile communication device that includes an interface circuit 506 that generates a chip enable signal enabling the flash ROM 502. See col. 6, lines 11-18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the mobile communication device of Costello and Christopherson by sending a chip enable signal from the interface circuit to the flash memory as taught by

Niiyama et al. to activate the flash memory in association with an address supplied from the

microprocessor.

Double Patenting

8.   Applicant is advised that should claim 1 be found allowable, claim 3 will be objected to

under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application

are duplicates or else are so close in content that they both cover the same thing, despite a slight

difference in wording, it is proper after allowing one claim to object to the other as being a

substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

9.   Claims 6-10 and 16-20 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims.

10.   The following is a statement of reasons for the indication of allowable subject matter: the

claims are objected to or allowed for the reasons stated in a previous Office action.

Response to Arguments

11.   Applicant's arguments with respect to the claims have been considered but are moot in

view of the new ground(s) of rejection.

        In light of further search, new grounds of rejection are applied to rejections of claims 4,

11-13 and 15.

Regarding claim 1, the claim does not recite that the second RAM stores temporary data generated while executing program data stored in a flash memory. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Moreover, although the second RAM stores data generated during the execution of program data, the claim does not recite that the generated data and the executed program data are connected in any way. Accordingly, Beckert's teaching of storing critical data in the SRAM reads on the claimed storing of generated data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Bhattacharya whose telephone number is (571) 272-7917. The examiner can normally be reached on Weekdays, 9-6, with first Fridays off.
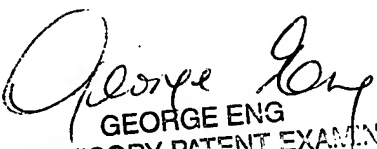
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, George Eng can be reached on (571) 272-7495. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

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like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sb

GEORGE ENG
SUPERVISORY PATENT EXAMINER